

Wireless Design Services

Business Model

Development Methodology

Design Gallery

PHYBIT

2008

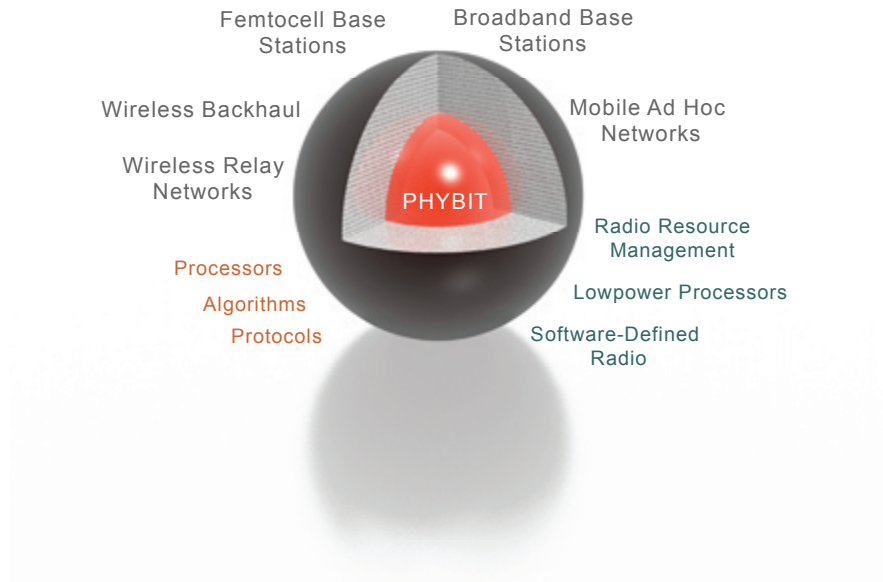
Welcome

Phybit provides advanced design services for a variety of wireless communications systems. Our work ranges from algorithms and protocols all the way to the development of production-quality systems on silicon.

Phybit core technology accelerates the development of wireless signal and protocol processors while meeting tight budget and schedule constraints. All our solutions are custom-made to match the specific and proprietary needs of our clients.

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Standard and Proprietary Systems

Phybit wireless design services are suitable for cost-effective implementation of complex functions in standard as well as proprietary systems.

System

Macrocell or Picocell Broadband Base Stations
 Femtocell and Home Base Stations
 Wireless Relay Stations
 Wireless Backhaul Equipment
 Wireless LAN Access Points
 Mobile Ad Hoc Networks

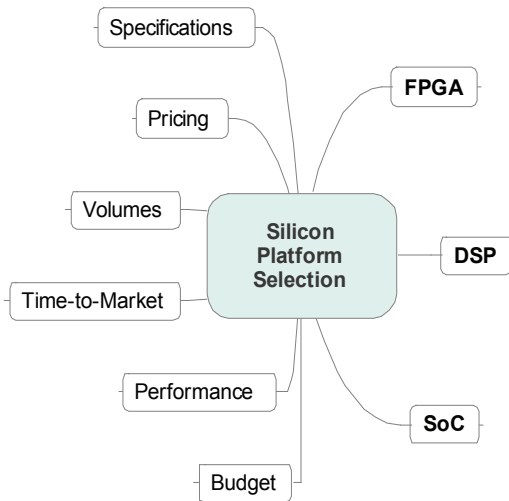
Standard

HSPA, LTE, WiMAX
 HSPA, LTE, WiMAX
 802.16j
 Proprietary, 802.16
 802.11n, VHT
 Proprietary, 802.11s

How We Work with Clients

Phybit Wireless Design Services

At Phybit, our development approach is the result of decades of experience in putting our skills to work to the full benefit of our exacting clients. We carry out every assignment in step-by-step ways and we believe that even the most complex problems have cost-effective solutions once they are broken down into smaller, simpler components.



From Algorithms to Silicon

Silicon Platforms for Wireless Systems

Economic considerations and competitive forces drive the development of wireless network equipment. Volumes make all the difference to how a solution is implemented in silicon and how it is deployed within and end-to-end system.

At Phybit, we consider all possible options in order to deliver the right solution to clients in timely and cost-effective ways. Depending on volume requirements, one or more of the options listed below.

Production Goals

Low Volumes

Mid Volumes

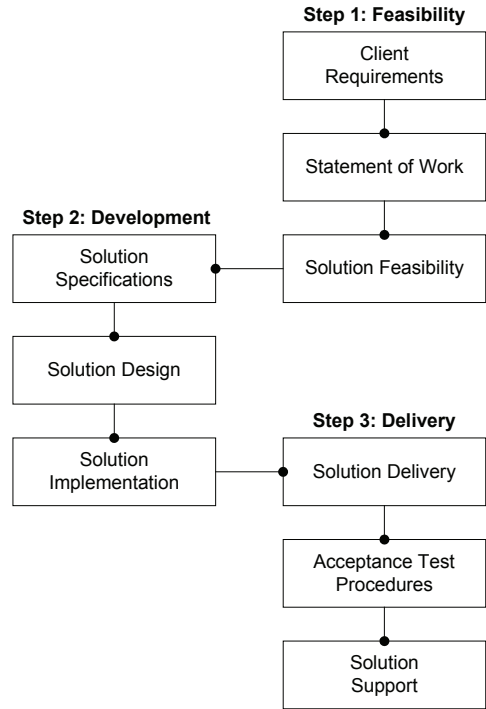
High Volumes

Silicon Platform

Field Programmable Gate Arrays (FPGA)

DSP, Programmable Processors, Structured ASIC

System-on Chip (SoC)



THREE STEPS TO SUCCESS

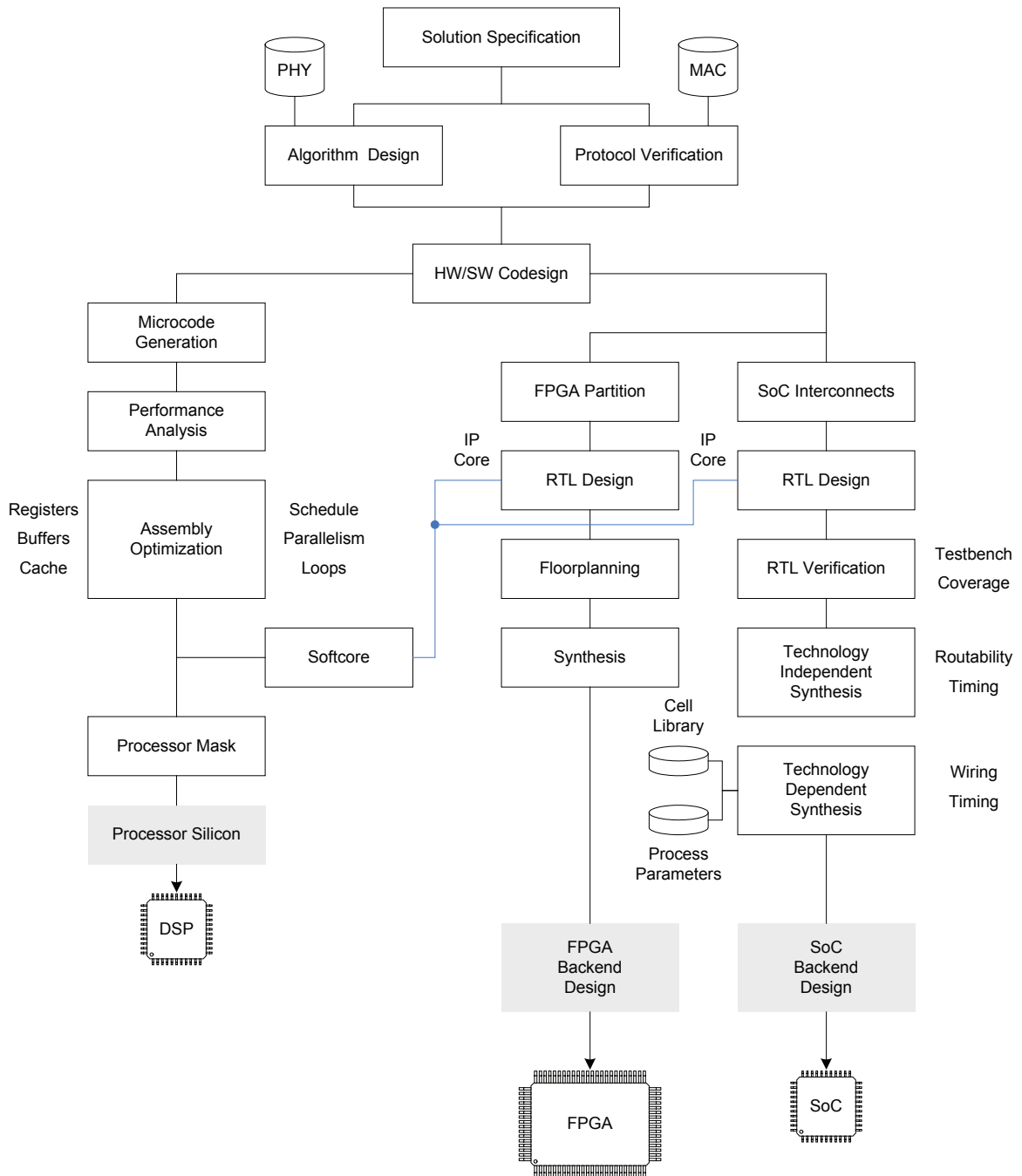
Phybit projects are typically carried out in three phase or steps in order to manage risks and provide clear-cut intermediate deliverables.

We begin a wish-list from clients to clearly specify the problem to be solved. The problems we face can range from a faster algorithm all the way up to a complex, multi-function system on silicon. We then outline a solution that makes sense to both clients and to ourselves before we proceed to formulate the specification of what the solution does, not how it does it. The how comes in a solution design step which describes in complete detail how the solution is to be implemented in silicon. This is followed by delivering the solution to our clients through a series of comprehensive acceptance test procedures with maximal coverage for quality assurance. After client acceptance, we proceed to support the solution as need may arise.

Phybit Frontend Design Services

Solution Development Methodology

Phybit focuses on the frontend of device development and we specialize in translating solution specifications into netlists for production-quality integrated circuits. As our projects always have both software programmable and hardwired components, we have developed an effective methodology for integrating softcores into both FPGA and SoC designs.

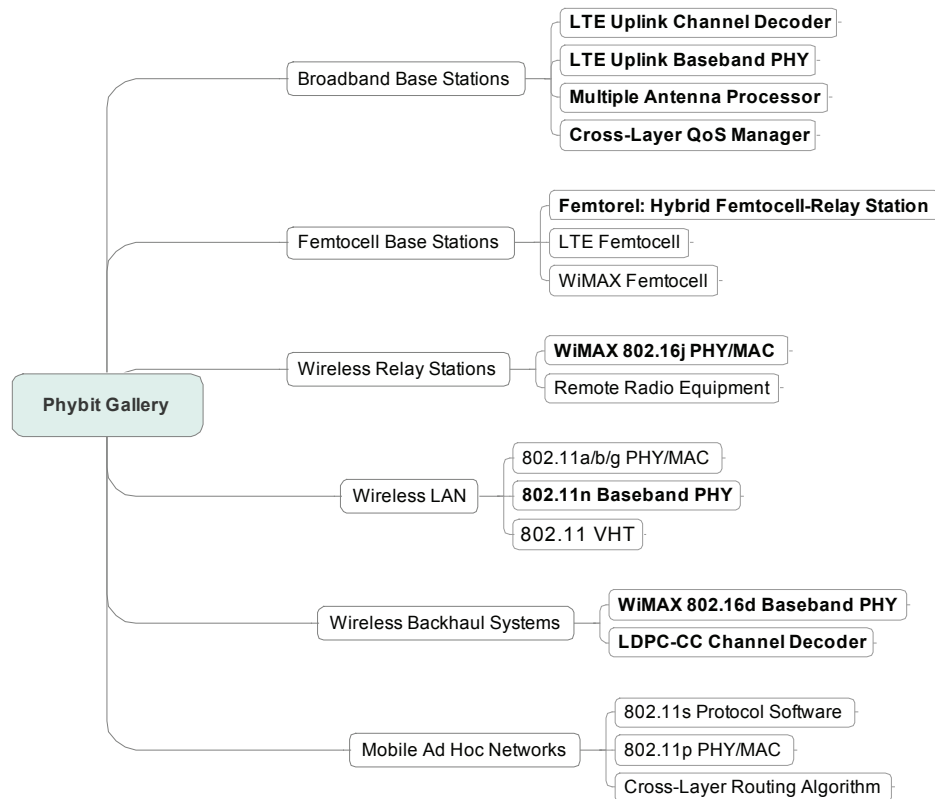


Phybit works with a select number of partners for backend FPGA and SoC services.

Design Galley

The following pages show a selection of our designs for PHY signal processing, and cross-layer MAC protocol functions. For each design, we describe the problem that must be solved, its solution, business applications, technical Features, and the commercial Benefits. We illustrate the performance that can be achieved by real-time implementation and sketch the key functional block diagrams of the final solution.

We hope these give insights into the extent of know-how that we put to use to solve techno-economic problems for our clients.



A Gallery of Phybit Designs

To illustrate the scope of our projects, we have selected a portfolio of designs for wireless applications as shown below. Further details are available upon request.

System	Phybit Design
Broadband Base Stations	LTE Uplink Channel Decoder LTE Uplink Receiver Multiple Antenna Processor Cross-Layer QoS Manager
Femtocell Base Stations	Hybrid Femtocell-Relay (Femto-rel) Station
Wireless Relay Stations	802.16j MAC/PHY
Wireless Backhaul System	802.16d PHY LDPC-CC Decoder
Wireless LAN Access Points	802.11n MiMo Receiver

Broadband Base Stations

LTE Uplink Channel Decoder

DESCRIPTION

Complete implementation of 3G Long-Term Evolution (Release 8) *Multiplexing and Channel Coding* functions as defined in 3GPP TS 36.212.

APPLICATIONS

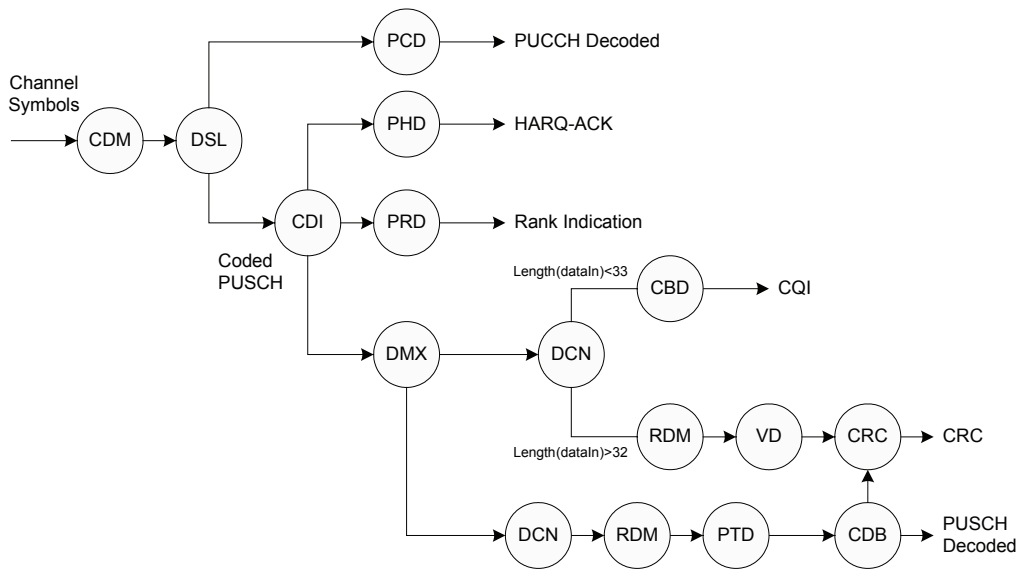
- LTE Channel Cards
- LTE Relay Stations
- LTE Test Equipment

FEATURES

- Software-based Interface by a Tiny RISC
- Partition into software and hardware
- Fully-parametric functions

BENEFITS

- Reduces base-station channel card costs



Acronyms

ACK = Acknowledgement
 CBD = CQI Block Decoder
 CDB = Code Block Desegmentation
 CDI = Channel DeInterleaver
 CDM = Channel DeMapper
 CQI = Channel Quality Indicator
 CRC = Cyclic Redundancy Check
 DCN = DeConcatenateNation
 DMX = DeMultipleXer
 DSL = Decode SeLector
 HARQ = Hybrid Automatic-Repeat-reQuest
 PCD = PuCch Decoder
 PHD = PUSCH HACK Decoder
 PRD = PUSCH RI Decoder
 PTD = PUSCH Turbo Decoder
 RDM = Rate DeMatcher
 RI = Rank Information
 VD = Viterbi Decoder

IMPLEMENTATION

Phybit LTE UL Channel Decoder can be implemented on FPGA chips in low volume quantities. It can fit into the following Xilinx parts:

- Virtex-5 LX
- Virtex-5 SXT
- Spartan-3
- Spartan-3A

We have included a tiny RISC processor in this design that takes up less than 500 Lookup Tables (LUTs), is programmable in C, and comes with the necessary software to control and set the parameters for all function blocks.

For mid to high volumes, it can be delivered as an ASIC.

DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates

FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

Broadband Base Stations

LTE Uplink Baseband PHY

DESCRIPTION

Complete implementation of 3G Long-Term Evolution (Release 8) uplink PHY from:

- 3GPP TS 36.201 *LTE Physical Layer General Description*,
- 3GPP TS 36.211 *Physical channels and modulation*
- 3GPP TS 36.213 *Physical layer procedures*
- 3GPP TS 36.214 *Physical layer measurements*

APPLICATIONS

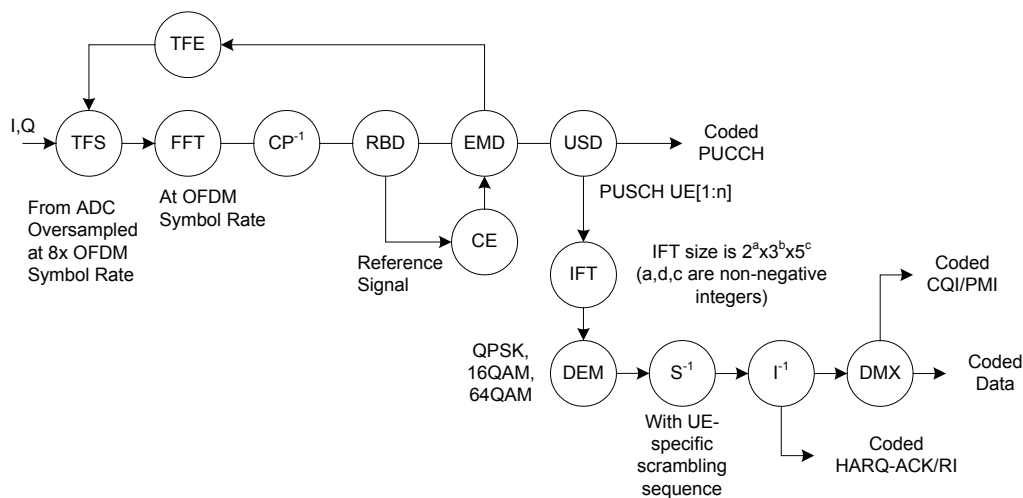
- LTE Channel Cards
- LTE Relay Stations
- LTE Test Equipment

FEATURES

- Software-based Interface
- Partition into software and hardware
- Fully-parametric functions

BENEFITS

- Reduces base-station channel card costs



Acronyms

CP⁻¹ = Cyclic Prefix Removal
 DMX = DeMultiplexer
 EMD = Equalizer & Multiuser Detection
 USD = UE Subcarrier Decoding
 I⁻¹ = De-Interleaver
 IFT = Inverse (Discrete) Fourier Transform
 PMI = Power Measurement Information
 RBD = resource Block Demapping
 S⁻¹ = Descrambler
 TFE = Time Frequency estimation
 TFS = Time Frequency Synchronization

IMPLEMENTATION

Phybit UL Baseband PHY is a complement to the UL Channel Decoder and the two solutions have the right interfaces to work together.

Through the use of a tiny 32-bit RISC processor, we have made it easy for system engineers to utilize all the resources and parameters of this solution through an Application Programming Interface (API). Details of this API plus an efficient design for interface to higher layers of LTE protocol stack are available upon request. These protocols include

- Medium Access Control (MAC) Layer (3GPP 36.321)
- Radio Link Control (RLC) Layer (3GPP 36.322)
- Packet Data Convergence Protocol (PDCP) Layer (3GPP 36.323)

DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

Broadband Base Stations

Multiple Antenna Processor

DESCRIPTION

This multiple antenna detection algorithm has much lower computational complexity than those based on QR decomposition. We have included signal processing functions to synchronize signals from each antenna, thereby allowing several local oscillators to be used for down-conversion.

APPLICATIONS

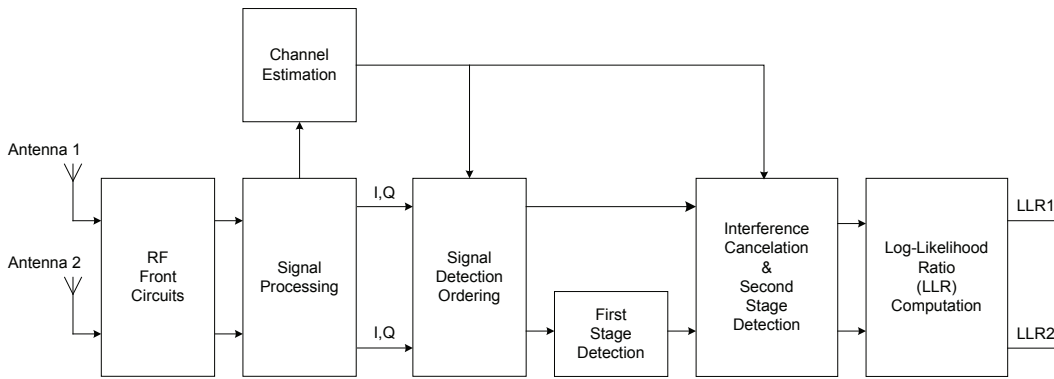
- LTE MiMo Detection
- WiMAX MiMo Detection
- 802.11n MiMo Detection

FEATURES

- Phybit's proprietary MiMo metric
- Synchronizes antenna signals
- Log-Likelihood Ratio (LLR) output
- Scalability with number of receiver antennas

BENEFITS

- Lowers development cost of MiMo receivers
- Simplifies radio circuits (use multiple LOs)
- The same algorithm works for any broadband standard



Phybit BLAST-Ordered List-Based MiMo Detector for 3GPP LTE

Acronyms

CE = Channel Estimation

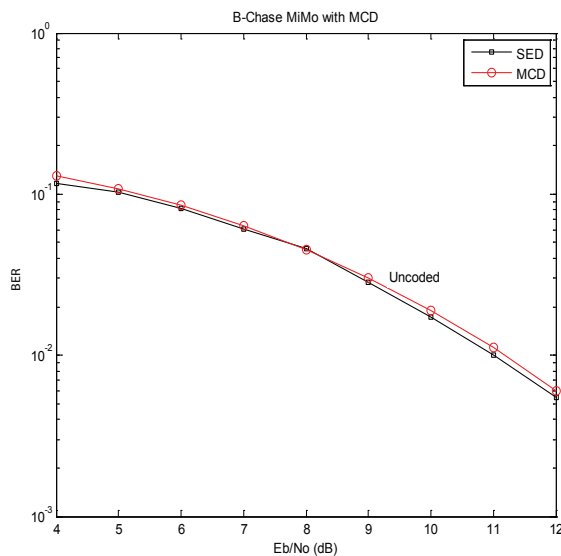
FSD = First-Stage Detection

LLR = Log-Likelihood Ratio

SDO = Signal Detection/Ordering

IMPLEMENTATION

This MiMo detector fits into any Xilinx Virtex-5 FPGA depending on the target application. Its Manhattan-Chase distance metric performs the same as Euclidean distance at a fraction of silicon power and area.



DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

Broadband Base Stations

Cross-Layer QoS Manager

DESCRIPTION

Phybit's Cross-layer QoS Manager combines measurements from both PHY and MAC layers to accurately compute a Channel Quality Indicator (CQI). The reliability metrics from a soft-decision decoder are mapped to an instantaneous measure of bit error probability, and statistical quality control (SQC) is applied to make BEP stable and stationary under practically any radio channel condition.

APPLICATIONS

QoS Management in:

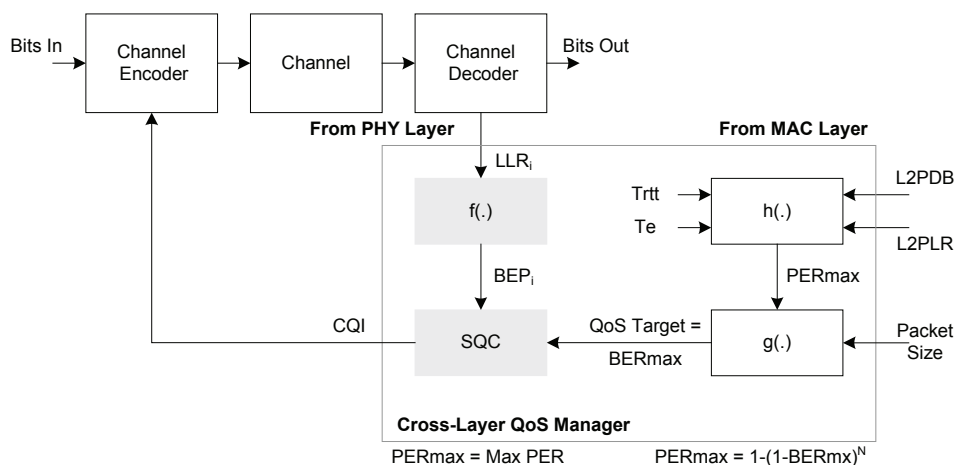
- VoIP over HSPA
- VoIP over LTE
- Mobile Broadband Video

FEATURES

- Instantaneous Bit Error Probability estimation
- Statistical Quality Control
- Layer 2 QoS parameters

BENEFITS

- Stable voice quality
- Stable video quality
- Improved coverage
- Higher capacity
- Stable throughput



Acronyms

- BEP = Bit Error Probability
- f(.) = Mapping Function 1
- g(.) = Mapping Function 2
- h(.) = Mapping Function 3
- LLR = Log-Likelihood Ratio
- L2PDB = Layer 2 Packet Delay Budget
- L2PLR = Layer 2 Packet Loss Ratio
- MAC = Media Access Control
- PER = Packet Error Rate
- PHY = Physical Layer
- QoS = Quality of Service
- Te = Elapsed Packet Life
- Trtt = Round-Trip Time

IMPLEMENTATION

The Cross-Layer QoS Manager fits into our L2IMP tiny 32-bit processor and can be readily integrated into HSPA and LTE baseband PHY designs. Simulations results show that the capacity of VoIP over HSPA can be doubled with even lower average delay per subscriber.

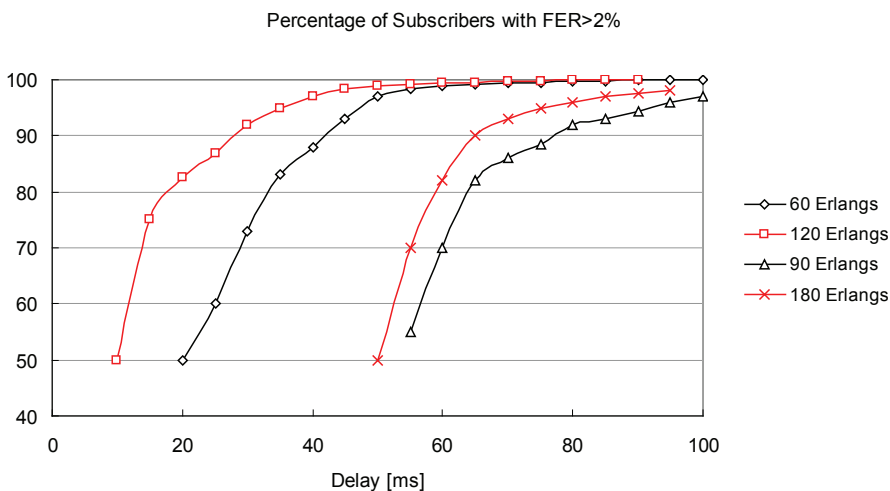
DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

L2IMP Design Package

- Assembly Source Code
- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench



Femtocell Base Station

Femto-rel: Hybrid Femtocell-Relay Station

THE FEMTO-REL CONCEPT

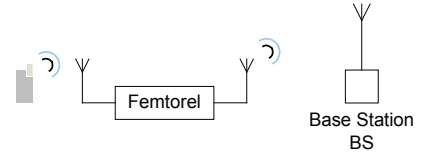
Femto-rel combines the best of relay stations with in-building base-station technology. It has three modes of operation

- As a relay-only station, it improves indoor coverage
- As a femtocell, it connects indoor subscribers to Internet
- As a hybrid device, it exchanges best-effort packets through a wired connection and communicates quality packets (VoIP, video) with the wireless network

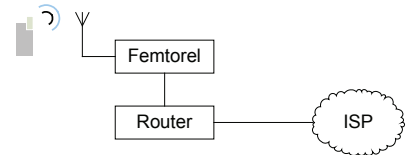
Femto-rel is an ideal component for the emerging Beyond 3G (B3G) networks as most of the latest standards such as LTE and WiMAX provide IP packets at the MAC layer. The classification of packet according to service quality can be done by MAC protocol, followed by routing to the appropriate destination.

FEMTO-REL CONFIGURATIONS

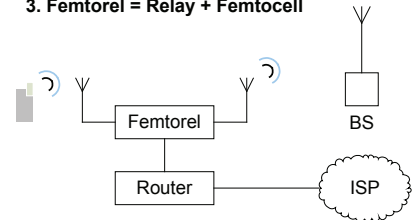
1. Relay Only



2. Femto-cell Only

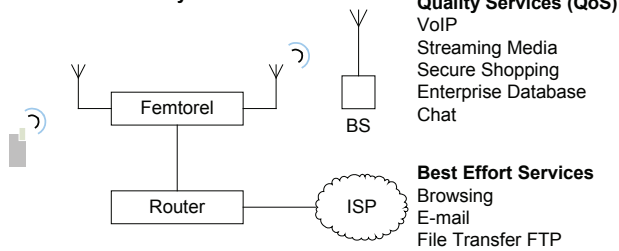


3. Femto-rel = Relay + Femto-cell

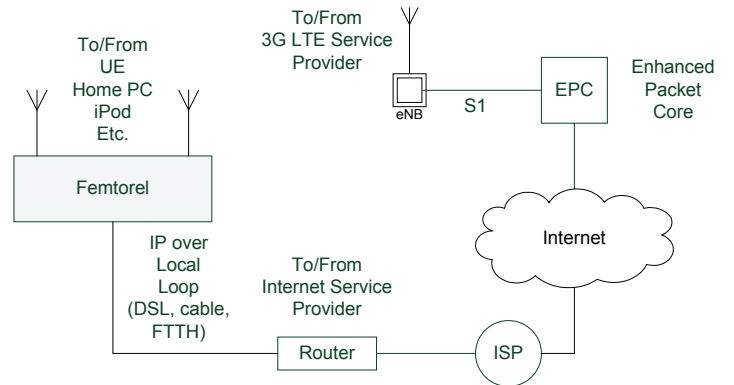


FEMTO-REL SERVICES

Hybrid Femto-cell-Relay Station



FEMTO-REL NETWORK INTERFACES

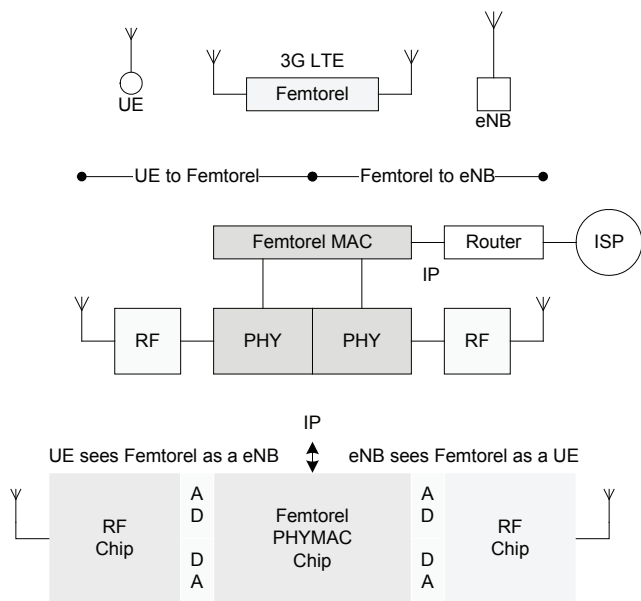


Femtocell Base Stations

Femto-rel: PHYMAC Processor

DESCRIPTION

Femto-rel PHYMAC is an integrated system-on-chip solution for Femto-rel. The device appears as a User Equipment (UE) to the base-station, and it appears as a base-station to a mobile station. Two sets of existing RF chips can be used to provide radio-in and radio-out interfaces. A simple Ethernet connection provides wired access.



APPLICATIONS

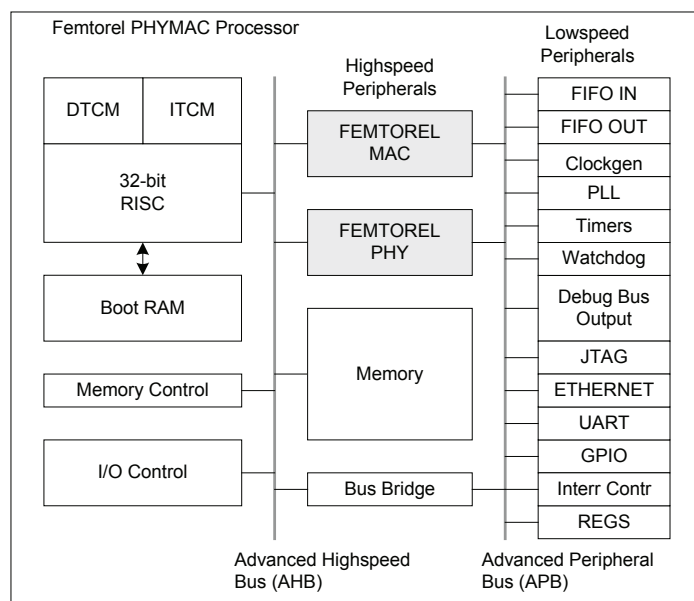
- LTE Femtocell
- LTE Relay station

FEATURES

- Phybit's patent-pending Femto-rel design
- Integrated PHY design
- Efficient MAC protocol

BENEFITS

- Improves coverage
- Enhances capacity
- Increases throughput



PHYMAC SYSTEM-ON-CHIP

Phybit can provide softcores for the MAC and PHY functions of Femto-rel for use in an SoC. We provide a complete design package to enable semiconductor device manufacturers or equipment developers to build integrated solutions for the Femto-rel concept.

DELIVERABLES

- Femto-rel System Design
- Femto-rel Link-Level Simulator
- Femto-rel System-Level Simulator
- Femto-rel Frequency Planner
- Femto-rel PHY Softcore
- Femto-rel MAC Softcore

Wireless Relay Stations

802.16j PHY

DESCRIPTION

Our 802.16j PHY implementation implements both uplink and downlink PHY functions for WiMAX relay station. We have used a programmable approach to reduce the risks of evolving standards.

APPLICATIONS

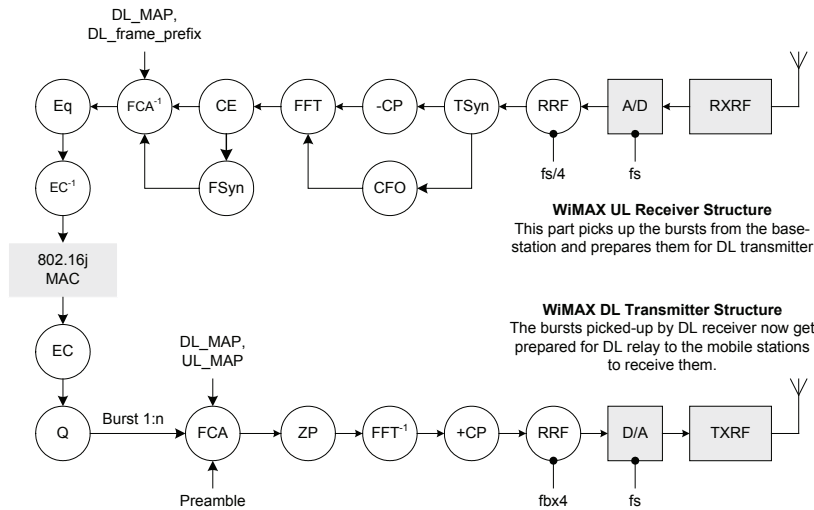
- WiMAX Relay Stations

FEATURES

- Integrated UL/DL all-digital PHY
- Efficient Ranging implementation
- High-performance Adaptive Equalizers

BENEFITS

- Improves coverage
- Enhances capacity
- Improves throughput



Acronyms

- A/D = Analog Digital Converter;
- CE = Channel Estimates;
- CP = Cyclic Prefix;
- D/A = Digital Analog Converter;
- EC = Error Control;
- Eq = Equalizer;
- FCA = Framing & Carrier Allocation;
- FFT = Fast Fourier Transform;
- FSyn = Frame Synchronization;
- RRF = Root Raised Filter
- Q = Quadrature Amplitude Mapper;
- TSyn = Timing Synchronization;
- ZP = Zero Pads (virtual carriers)

IMPLEMENTATION

Our 802.16j PHY fits into two H2ASVP softcores. For signal demodulation and equalization, one H2ASVP.

For channel decoding decoder, Phybit H2FEC core can be used.

DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

Phybit H2ASVP Design Package

- Vectorized Assembly Code
- H2ASVP Softcore Netlist

H2ASVP+H2FEC FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

Wireless Relay Stations

802.16j MAC

DESCRIPTION

Phybit 802.16j MAC is divided into Upper and Lower parts. Upper MAC handles Distributed and Centralized scheduling, plus. The MAC can also work in both transparent and non-transparent modes. Lower MAC provides radio resource management and a very efficient interface to PHY.

APPLICATIONS

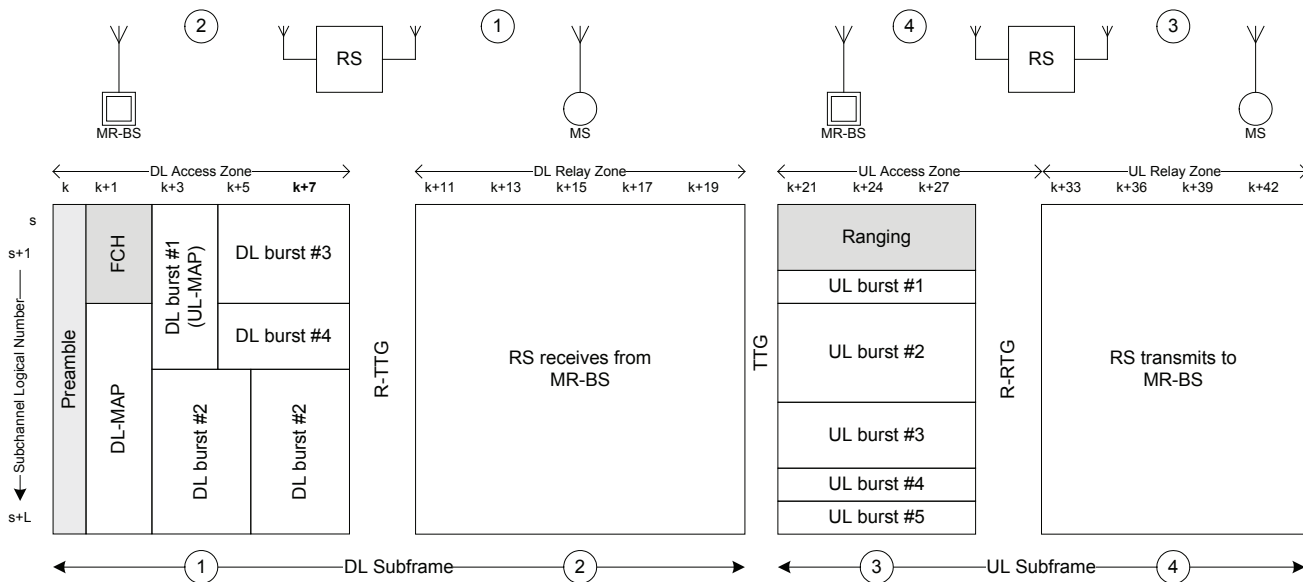
- WiMAX Relay Stations

FEATURES

- Supports both Centralized or Distributed Scheduling
- Handles both transparent or non-transparent modes
- Advanced radio Resource Allocation
- Efficient Lower MAC (MAC-PHY) Interface

BENEFITS

- Improves coverage
- Enhances capacity
- Improves throughput



IMPLEMENTATION

Phybit 802.16j MAC fits into one L2PRO softcore for the upper MAC and one L2IMP for the lower MAC.

DELIVERABLES

- MAC Performance Simulator
- Phybit L2PRO and L2IMP Design Package
- Optimized C/Assembly Code
- L2IMP Softcore Netlist
- L2IMP Softcore Netlist

Wireless Backhaul

WiMAX 802.16d Baseband PHY

DESCRIPTION

An efficient baseband design for IEEE Std 802.16-2004 WirelessMAN PHY.

APPLICATIONS

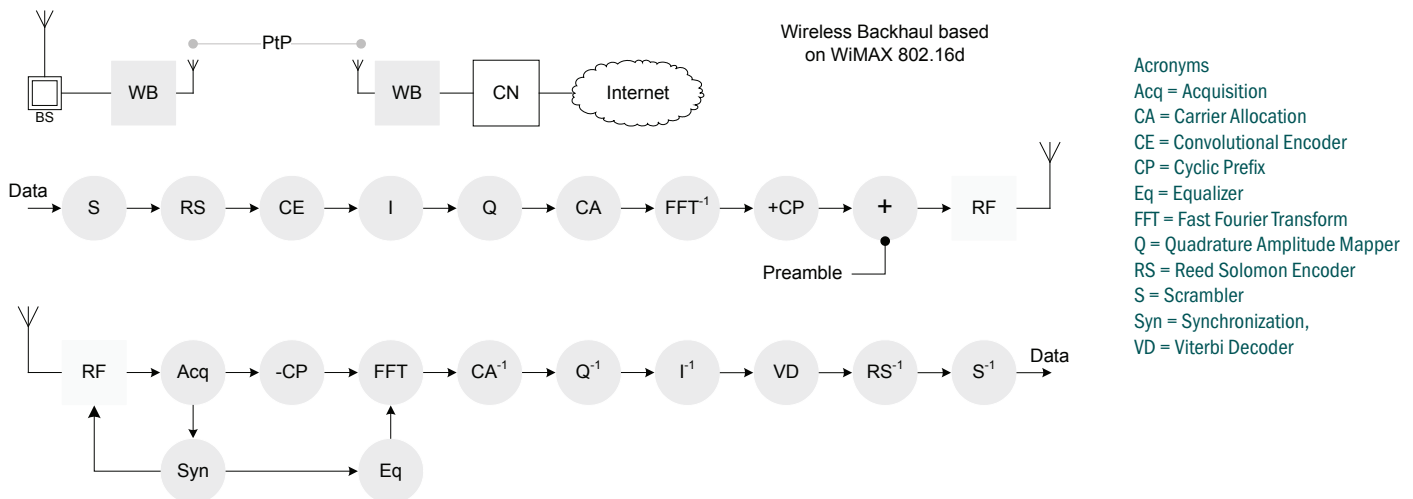
- Point-to-Point Wireless
- Wireless Backhaul Systems
- Wireless Internet Service Provision

FEATURES

- Unique soft-decision RS decoder (patent-pending)
- Fully-programmable softcores

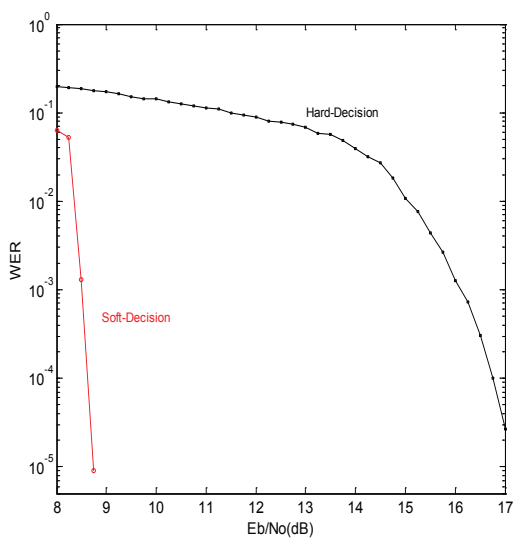
BENEFITS

- Improves coverage
- Enhances capacity
- Improves throughput



IMPLEMENTATION

Our 802.16d PHY fits into two H2ASVP softcores. For signal demodulation and equalization, one H2ASVP. For our unique soft-decision Reed-Solomon (RS) decoder, Phybit H2FEC core can be used.



DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

Phybit H2ASVP Design Package

- Vectorized Assembly Code
- H2ASVP Softcore Netlist

RS Decoder FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

Wireless Backhaul

LDPC-CC Decoder

DESCRIPTION

An efficient channel decoder for LDPC Convolutional Codes. These are a class of Shannon approaching codes with the advantage of handling variable block sizes: an ideal feature for Adaptive Modulation and Coding (AMC).

APPLICATIONS

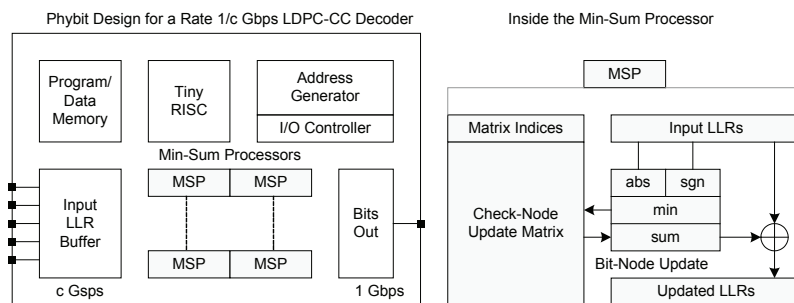
- Point-to-Point Wireless
- Wireless Backhaul Systems

FEATURES

Efficient Min-Sum Processor
Efficient Address Generation
Highly Parallel Implementation
Giga-rate Execution

BENEFITS

- Improves coverage
- Enhances capacity
- Improves throughput

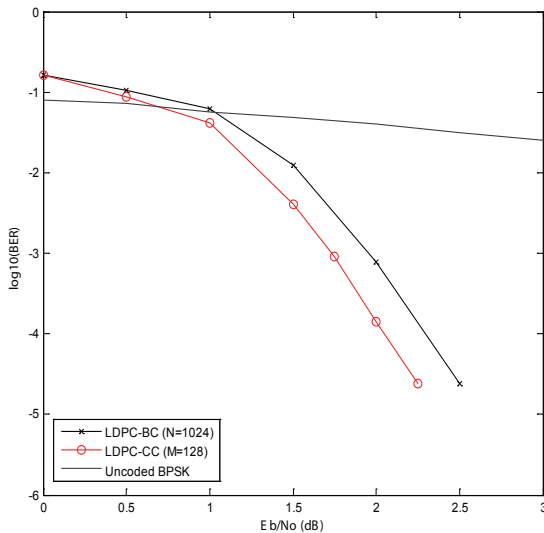


IMPLEMENTATION

The LDPC-CC design fits into Phybit H2FEC softcore.

PERFORMANCE

our fixed-point, soft-decision LDPC-CC decoder outperforms block codes of much higher complexity and comes close to the Shannon limit.



DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

Phybit H2FEC Design Package

- Vectorized Assembly Code
- H2FEC Softcore Netlist

RS Decoder FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

Wireless LAN

802.11n MiMo Receiver

DESCRIPTION

- A complete design for the baseband PHY of IEEE 802.11n Draft 5.0 (July 2008).

APPLICATIONS

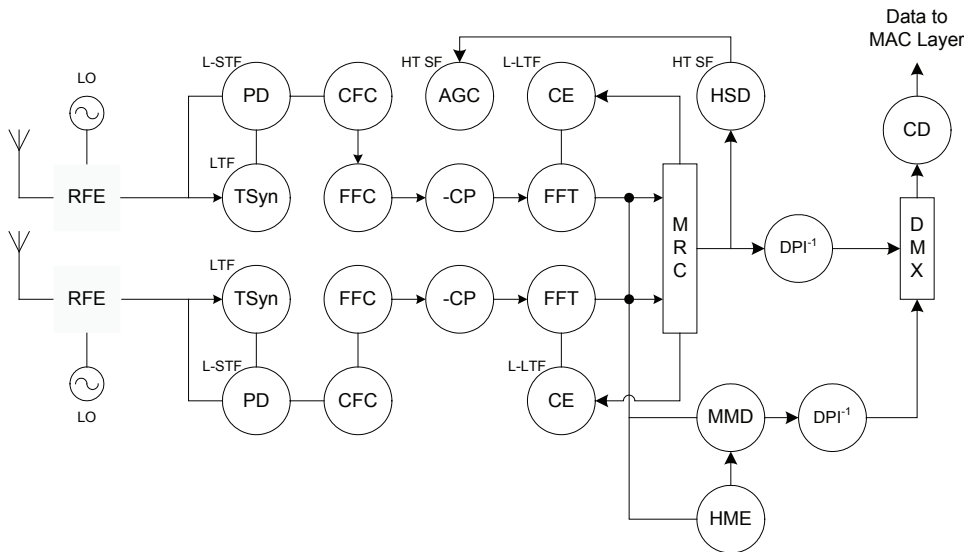
- High-throughput Wireless LAN

FEATURES

- Phybit proprietary MiMo metric
- Multiple programmable softcores
- Efficient MAC interface
- Backward compatibility with 802.11a/b/g

BENEFITS

- Rapid development of 802.11n chipsets



Acronyms

Acq	=	Acquisition
AGC	=	Automatic Gain Control
CD	=	Channel Decoder (Viterbi)
CE	=	Channel Estimator
CDC	=	Coarse Frequency Correction
CP	=	Cyclic Prefix
DPI	=	De-mapper/Puncture/Interleaver
DMX	=	De-Multiplexer
Eq	=	Equalizer
FFC	=	Fine Frequency Correction
FFT	=	Fast Fourier Transform
HME	=	H-Matrix Estimator
HSD	=	HT SF Detector
LO	=	Local Oscillator
P	=	Puncture
PD	=	Packet Detection
MMD	=	MiMo Detector
RFE	=	Receiver Front-End
TSyn	=	Time Synchronization

IMPLEMENTATION

Phybit 802.11n MiMo receiver design is based on multiple softcores, each being a programmable H2ASVP optimized for a subset of PHY functions. Specifically, there are four H2ASVP softcores in this design;

- H2ASVP MiMO Softcore
- H2ASVP Synchronization Softcore
- H2ASVP OFDM Demodulation and Equalization
- H2ASVP Acquisition Processor

All four softcores fit into Virtex-5 SXT FPGA.

DELIVERABLES

Fixed-Point C simulator

- Source Code
- Algorithm Documentation
- Float vs. Fixed Error Rates (uncoded)

Phybit H2ASVP Design Package

- Vectorized Assembly Code
- H2ASVP Softcore Netlist

RS Decoder FPGA Design Package

- RTL Synthesizable VHDL
- Routing and Timing Data
- Unified Constraint File (UCF)
- Bitstream
- Netlist
- Testbench

The Wireless World

Phybit Design Services

SYSTEMS

Broadband Base Stations
Femtocell Base Stations
Wireless Relay Systems
Wireless Backhaul
Wireless LAN
Mobile Ad Hoc Networks

SERVICES

Algorithm Design
Protocol Implementation
Embedded Software Development
FPGA Implementation
System-on-Chip Development

FEATURES

Re-usable PHY Algorithm Library
Re-usable Protocol Software
Proven, Pre-Made Designs

BENEFITS

Faster Time-to-Market
Lower Development Cost
Higher Performance
Lower Production Cost
Lower Maintenance Cost



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