

Wireless Products

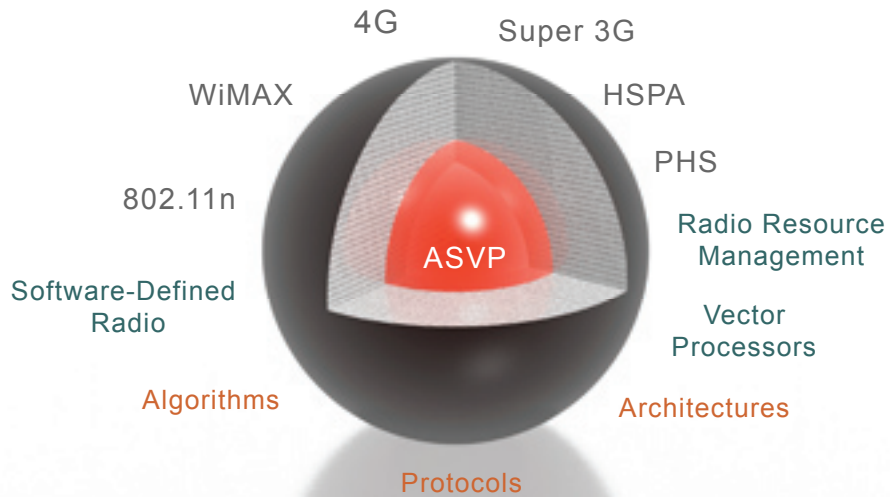
Processor Architectures
Physical Layer Algorithms
Multistandard Protocols

PHYBIT

Welcome

At Phybit we have a pure focus on mobile broadband systems and our mission is to bring the right products to the market fast. To achieve this goal, we develop protocol and signal processors whose features and resources match the massive computational requirements of worldwide standards such as 3GPP Long-Term Evolution (LTE) and WiMAX.

This catalogue provides an overview of Phybit solutions. It lists the technical features and the business benefits of our unique products and it shows how our hardware processors are backed-up by a wide range of software for signal computing and network protocols. After all, what is hardware without software?



At Phybit, we develop advanced microarchitectures to handle massive signal computing in real time. We focus on standard wireless systems and on emerging networks based on long term evolution of 3G, WiMAX and 4G.

We deliver algorithms, protocols, and architectures for higher capacity, wider coverage, longer battery life, lower access delays, faster throughput, and lower costs.

Phybit solutions offer the full versatility and time-to-market advantages of programmable processors. We combine optimal algorithms with the latest parallel processors on silicon to provide flexibility and ease-of-upgrade over single-function, hardwired signal processors.

H2

Dual Digital Signal Processor

H2 is a 16-bit DSP core for 3G Physical Layer signal processing. It is suitable for WCDMA at data rates of up to 2 Mbps, and is delivered as Synthesizable VHDL plus Testbench, Netlist, or as GDSII files.

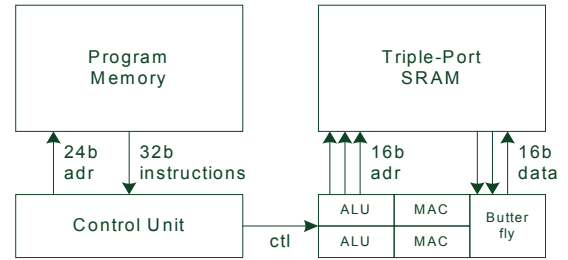
FEATURES

H2 has a small size 75,000 gates without memory, a 7-stage pipeline with dual execution stages, Two 48-bit accumulators + one 32-bit accumulator, Two 16bx16b multipliers in signed/unsigned modes, and supports Triple-Port RAM access.

BENEFITS

H2 is easy to program and maintain, it is suitable for rapid integration into SoC or Many-core chips, and its low power consumption increases battery life.

Phybit H2 Harvard Architecture



ALU datapath is optimized for 3G physical layer, and Viterbi decoding:
 N/2 cycles for N-tap FIR
 4-cycle Radix-2 FFT Butterfly
 1-cycle Viterbi decoder butterfly

H2ASVP

Application-Specific Vector Processor

H2ASVP is a Vector processor optimized for PHY modulation and demodulation. It is the vector version of H2 and its highly regular microarchitecture makes it easy to program with vector data types. At 200 MHz, it gives 3200 MIPS for 16-bit data and 6400 MIPS at 8-bits.

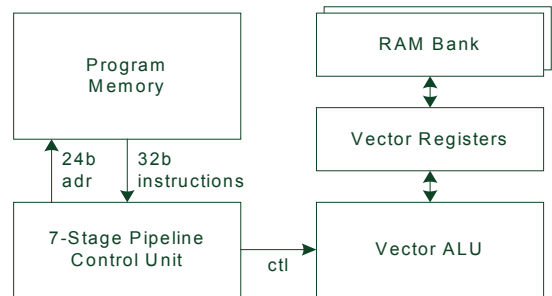
FEATURES

Specific instructions or fast, lowpower implementation of FFT, FIR, and demodulation functions.

BENEFITS

Enables single-chip implementation of mobile broadband physical layer.

Phybit H2ASVP Architecture



Optimized for PHY Demodulation; fast FIR and FFT

H2FEC

Programmable Channel Decoder

H2FEC is a vector processor optimized for soft-decision, factor-graph decoding of turbo, LDPC, and convolutional decoders. At 200 to 300 MHz, it matches the processing requirements of mobile broadband standards such as 3G LTE and WiMAX by providing 30 to 50 Mbps throughput for decoded data.

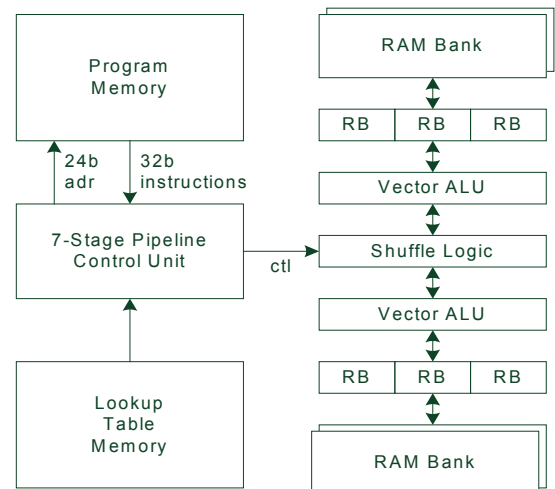
FEATURES

H2FEC has a datapath for fast execution of factor-graph decoding algorithms and has a small size of less than 400,000 gates.

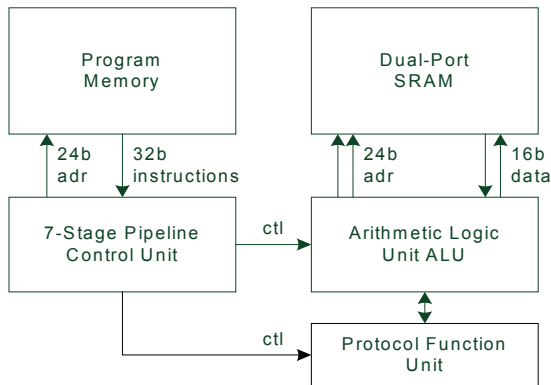
BENEFITS

Eliminates the need for expensive hardwired implementation of mobile broadband channel decoders. Reduces system costs and development budgets.

Phybit H2FEC Architecture



Phybit L2PRO Harvard Architecture



L2PRO

Lowpower Protocol Processor

L2PRO is a 32-bit RISC processor with specific instructions for efficient, lowpower implementation of mobile broadband protocol stacks. The instruction set architecture of L2PRO matches Layer 2 processing functions of standards such as 3G LTE and WiMAX 802.16e.

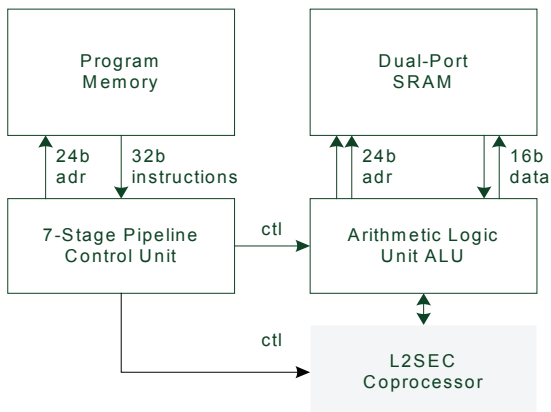
FEATURES

A Protocol function Unit that provides specific instructions for Random Number Generation, CRC, Counters, Timers, and Bitstring Matching.

BENEFITS

Saves project time and budget by accelerating the development and testing of protocol stacks for mobile broadband standards.

Phybit L2SEC Coprocessor



L2SEC

Security Coprocessor

L2SEC is a programmable coprocessor for software implementation of security protocols based on Integer Factorization (IF), Discrete Logarithms (DL), and Elliptic Curve Discrete Logarithms (ECDL). It provides efficient hardware support for Public Key algorithms and Number Theoretic cryptography.

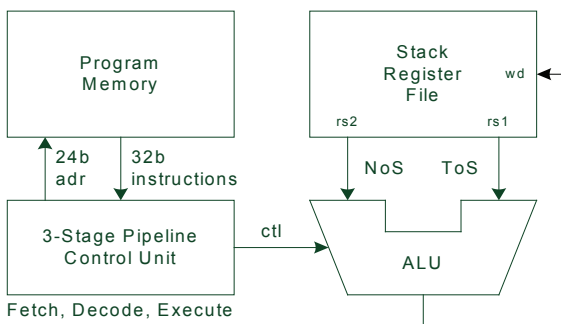
FEATURES

L2SEC has a cryptographic arithmetic unit with specific instructions for Modular Exponentiation ($a^b \text{ mod } N$), Finite Field Exponentiation, and Elliptic Curve Arithmetic (Doubling, Addition, and Multiplication).

BENEFITS

L2SEC eliminates the cost of developing hardwired cryptography circuits. L2SEC Can be used with any RISC processor to accelerate the execution of security protocols.

Phybit L2IMP Coprocessor



L2IMP

Idle Mode Processor

Mobile Broadband devices spend most of their lifetime in idle mode, checking network status and waiting to be called (paged). Phybit's Idle Mode Coprocessor is a tiny 32-bit RISC processor designed for efficient processing of idle mode tasks in wireless terminals. It has specific instructions for decoding paging channels so as to relieve the main protocol processor from becoming involved in the idle mode and thereby save precious power.

FEATURES

A tiny, stack-based RISC microarchitecture with an instruction set architecture matched to the Idle Mode functions of mobile broadband standards.

BENEFITS

Enhances battery life of mobile broadband devices.

ALGORITHM LIBRARY

Multistandard Physical Layer Functions

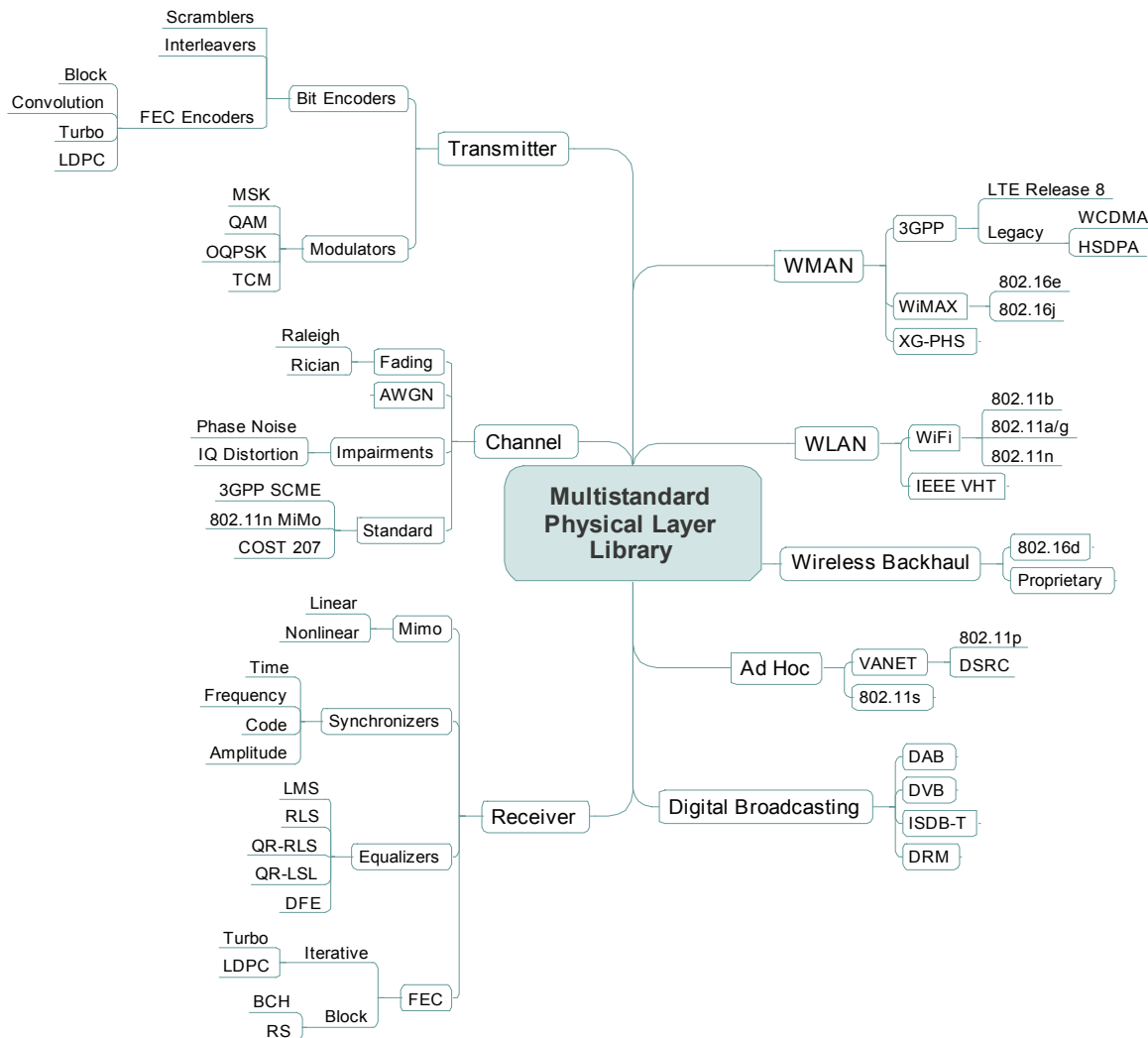
Phybit offers the largest collection of physical layer (PHY) algorithms under one roof. The signal processing functions that work together to make up end-to-end physical layer algorithms are organized according to where they are used, plus to which standards they suit. The net result is fast, industrial-quality PHY solutions for multiple mobile broadband standards.

FEATURES

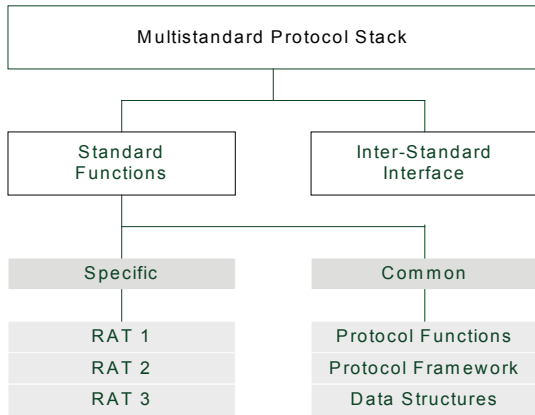
- Modular and hierarchical organization of physical layer functions for a largest set of mobile broadband standards.
- Fixed-point arithmetic for rapid translation to target real-time hardware.
- Performance above and beyond the bit error rate requirements of mobile broadband standards.

BENEFITS

- Accelerates the development and real-time implementation of physical layer solutions for mobile broadband standards.
- Helps to reduce development costs.



Phybit MAC Library Structure



RAT
Radio Access Technology

e.g.
RAT1 WiMAX,
RAT2 3G LTE
RAT3 XG-PHS

PROTOCOL SOFTWARE

Multistandard Protocol Stack

Phybit has developed a generic framework for real-time implementation of wireless protocol stacks that can be used for any mobile broadband standard. Our Multistandard Protocol Stack (Phybit MPS) can be used to develop efficient standard-specific data link layer solutions, or it can be used as a multi-mode protocol software that handles several standards at the same time.

FEATURES

A unified set of common plus standard-specific protocol functions that handle any radio access technologies.

BENEFITS

Rapid development of multi-mode protocol stacks for multistandard terminals, small base stations, and access points.

PHYBIT MPS FUNCTIONS

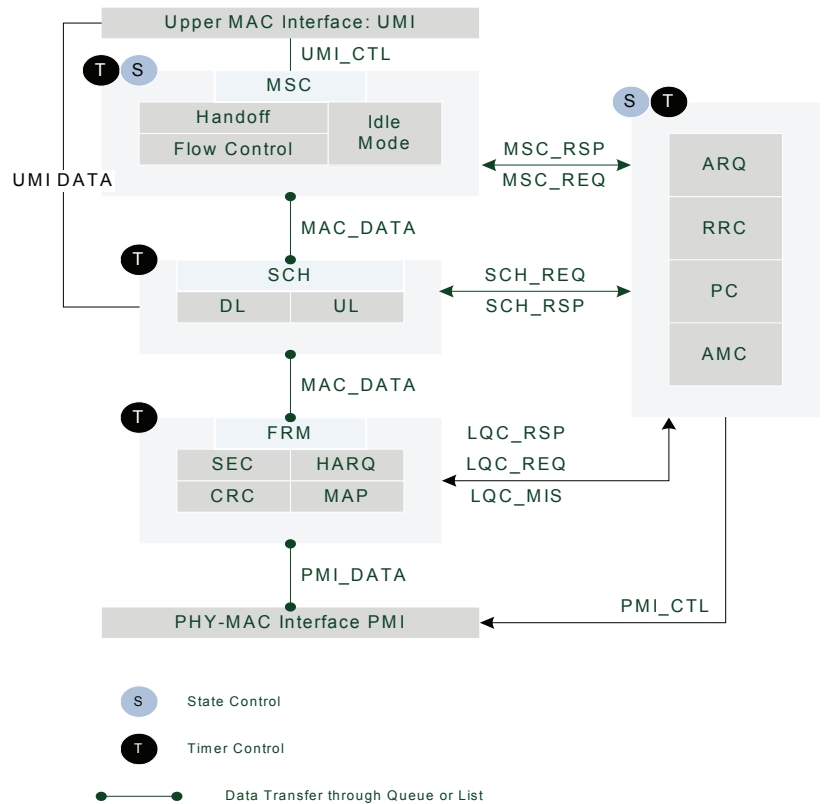
The functions provided by Phybit MPS are in four classes:

- FRH: Frame Handler Class
- SCH: Scheduling Class
- MSC: Message Service Control Class
- LQC: Link Quality Control Class

The diagram on your right shows the overview of the interactions in between these classes. PMI (PHY-MAC Interface) consists of a group of functions that are responsible for transferring data messages and control signals between PHY and MAC layers. Similarly, UMI (Upper-layer MAC Interface) consists of a group of functions for data message and control signal to-and-from the MAC layer and upper layers.

All the communication between PHY and MAC layers are through mail-box exchange mechanisms. This separates the PHY and MAC processors and ensures that the MAC layer works with any PHY hardware. Whenever data is written into the mail-box, interrupt will occur through a general-purpose input/output port to inform the destination processor that data is available.

Phybit MAC Library Functions



PHYBIT

**Architectures, Algorithms, and Protocols
for Wireless Communications**

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